

INTEGRATED DEVICE CIRCUIT, ELECTRONIC UNIT FOR SMART  
CARDS USING SAID DEVICE AND METHOD FOR MANUFACTURING  
SAID DEVICE

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**FIELD OF THE INVENTION**

The present invention relates to an integrated circuit device, an electronic unit for smart cards using the integrated circuit device and a method for manufacturing said device.

More specifically, the present invention relates to the manufacturing of a semiconductor chip in which integrated circuits are formed, having a structure such that electronic units for smart cards of reduced thickness can be manufactured.

**BACKGROUND OF THE INVENTION**  
It is known that smart cards used in particular as banking cards, such as an identification card, or also as a payment card for different services, are essentially made of a plastic material body of rectangular parallelepiped shape in which is inserted an electronic unit most often made of a semiconductor chip attached to an insulating substrate provided with external electrical contact pads. These external pads enable electrical connection between the circuits in the semiconductor chip and circuits in a read-write device when the card is inserted within such a device.

According to the prevailing standards, the card body should have a thickness of about 0.8 mm. It should be understood that the thickness of the electronic unit is therefore one of its critical parameters, and facilitates the insertion of the electronic unit within the card body and ensures a proper mechanical coupling between the card body and the electronic unit as well as the mechanical integrity of the electronic unit.

In the appended Figure 1, a vertical cross section of an electronic unit for smart cards made according to a known technique is shown. Electronic unit 10 is essentially comprised of a semiconductor chip 12 in

which integrated circuits are formed, this chip having an active face 14 provided with electrical connection terminals 16. The semiconductor chip 12 is attached to an insulating substrate 18 through an adhesive layer 19.

5 The external face 18a of the insulating substrate is provided with external contact pads 20 to be contacted with the electrical contacts of the read-write device. Terminals 16 of chip 12 are connected to external pads 20 through leads such as 24. According to a known

10 method, the

insulating substrate comprises windows 26 with electrical leads 24, so that the use of a doubled-faced printed circuit is avoided. In order to ensure electrical integrity of chip 12 and electrical leads 24, they are encapsulated with an insulating material 26 such as an epoxy resin.

In some cases, the wire leads can be replaced with other electrically conducting elements for connecting the chip terminals to external pads on the insulating substrate.

With such a manufacturing technology, an electronic unit having an overall thickness of about 0.6 mm, is obtained, to be compared with the 0.8 mm thickness of the card body.

Techniques that would allow reducing this thickness are difficult to implement. They could consist in reducing the chip thickness, which is conventionally of the order of 180  $\mu$ m, but this would unacceptably reduce chip strength. One could also reduce the thickness caused by the curvature of electrical wires 24 or similar electrical connection elements. This, however, requires using the so-called "Wedge bonding" technology which is of costly implementation. Finally, it could be contemplated to reduce the thickness of the insulating resin of encapsulation 26. Such a reduction would however reduce the strength of the electronic unit as a whole.

#### **SUMMARY OF THE INVENTION**

US 5,155,068 discloses a method of manufacturing an electronic unit for smart cards. According to this method a semiconductor chip comprises an active face provided with metallic wire layers. Connections are formed between these metallic wire layers and a substrate provided with electrical contacts. An acryl or epoxy resin is then applied for attaching the semiconductor chip to the substrate with its electrical contacts. The method is of costly implementation.

A first objet of the present invention is to provide an integrated circuit device permitting the

manufacturing of an electronic unit for smart cards having a reduced thickness while not having the drawbacks of the above-mentioned techniques.

To achieve this object, according to the invention,  
5 the integrated circuit device is characterized in that it comprises:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical  
10 connection terminals and a second face, wherein the chip has a thickness of less than 100  $\mu\text{m}$ , and

- a complementary chip having a first face attached to the active face of the active chip, a second face and a side surface, wherein the complementary chip has a  
15 plurality of recesses, each recess extending through the whole thickness of the complementary chip and extending from above a contact terminal to said side surface.

An electronic unit for smart cards can be realized from such an integrated circuit device. The electronic  
20 unit further comprises an insulating substrate having an outer face provided with outer electrical contact pads and an inner face, the second face of the active chip being attached to the inner face of the substrate, and a plurality of electrical leads, each lead having a first  
25 end connected to a contact terminal and a second end connected to an external contact pad and lying entirely between the plane containing the second face of the complementary chip and the insulating substrate.

It should be understood that, due to the reduced  
30 thickness of the active layer, on the active face of which contact terminals are formed, these contact terminals are close to that face of the integrated circuit device which is attached to the insulating substrate when the electronic unit is formed. It should  
35 also be understood that, due to the presence of recesses which open into the side surface of the complementary layer, it is possible, when forming the electronic unit, to provide connection in the electric wires which are

integrally provided below the plane that includes the upper face of the complementary layer. It should be understood that the resulting thickness of the electronic unit is substantially reduced relative to the thickness of an electronic unit of the previously described type.

The present invention also relates to a method for manufacturing an integrated circuit device from:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, and

- a complementary chip having a first face, a second face and a side face, the complementary chip including a plurality of recesses, each recess extending through the whole thickness of the complementary chip, wherein the method is characterized in that it comprises the following steps:

- an attachment step wherein the first face of the complementary chip is attached to the active face of the active chip so that a recess of the complementary chip extends from above a contact terminal of the active chip to the side surface of the complementary chip; and

- an etching step wherein the active chip is etched from its second face so as to provide it with a thickness of less than 100  $\mu\text{m}$ .

It should be understood that according to this method, the starting element is an active layer having a standard thickness, namely about of 180  $\mu\text{m}$ , which active layer is attached to the complementary layer, which itself has a certain thickness. Thus, an assembly is obtained with a sufficient thickness for etching the non-active face of the active layer while complying with overall dimensions such that the assembly maintains a sufficient mechanical strength.

Other features and advantages of the present invention will be apparent from the following detailed description of an embodiment of the invention given by way of non limiting example in reference to the accompanying drawings in which:

**BRIEF DESCRIPTION OF THE DRAWINGS**  
Figure 1, already described, shows a vertical cross-section of an electronic unit for a standard smart card.

Figures 2a and 2b show a vertical cross-section of two manufacturing steps of the electronic unit according to this invention;

Figure 3 shows a horizontal cross-section of the electronic unit along line III-III of Figure 2b; and

Figures 4a to 4c show the various steps of the method for manufacturing the integrated circuit device.

**DETAILED DESCRIPTION**  
Referring first to Figures 2 and 3, a description will be given of the integrated circuit device or electronic chip and the electronic unit using the same.

**DETAILED DESCRIPTION**  
The integrated circuit device 30 is essentially comprised of an active layer 32 of a semiconductor material, typically silicon, into which the different integrated circuits are formed. This active layer 32 has an active face 34 into which electric contact terminals and an attachment face 38 are formed. The integrated circuit 30 also comprises a complementary layer 40 whose first face 42 is attached through any appropriate means, for example, an intermediate sealant layer formed of a polyimide, to the active face of active layer 32 and whose upper face 44 is free. Complementary layer 40 may also be advantageously made of silicon, but other materials having physical characteristics similar to silicon, in particular in what concerns its thermal expansion coefficient, could be used. One of the functions performed by complementary layer 40 is to form a protective layer against fraud attempts that could be performed with respect to the active layer integrated circuits.

As more clearly shown in Figure 3, complementary layer 40 is provided with recesses such as the one shown in 46 (in the given example, there are five connection terminals 36 and five recesses 46). Each recess 46  
5 extends over the whole thickness of the complementary layer and extends from contact terminal 36 to the side surface 48 of complementary layer 40. In other words, these recesses open laterally into the complementary layer.

10 According to the above described embodiment, the thickness  $e_1$  of the complementary layer is 140  $\mu\text{m}$  and the thickness  $e_2$  of the active layer is 40  $\mu\text{m}$ . Thus, the total thickness of the integrated circuit device is 180  $\mu\text{m}$ , which corresponds to the thickness of a standard  
15 semiconductor chip.

More generally, the thickness of the active layer is less than 100  $\mu\text{m}$ , which reduced thickness can be obtained by resorting to the manufacturing method described below. Still preferably, thickness  $e_2$  of the  
20 active layer ranges from 5 to about 50  $\mu\text{m}$ .

The thickness of the active layer is thus significantly greater than that of the semiconductor chip. In particular, this leads to a thinner unit, since the lead wires are effectively located, according to a  
25 preferred embodiment of the present invention, within the overall thickness of the assembly formed by the complementary layer and the semiconductor chip that constitutes the active layer.

The complementary layer covers substantially  
30 entirely or entirely the active face of the active layer except, of course, for the recesses. More specifically, the surface area of the active face of the active layer is substantially the same as the surface area of the first face of the complementary layer after subtracting  
35 the surface area corresponding to the recesses formed in said complementary layer. Therefore, it is possible to process the active layer so as to reduce its thickness down to the desired value. In addition, the active

layer/complementary layer assembly is more resistant to the mechanical strains it may undergo, since the complementary layer protects the active layer.

Moreover, it should be noted that there are  
5 advantageously as many recesses as connection terminals in the semiconductor chip and that such recesses represent a reduced portion of the total surface area of the complementary layer.

For forming the electronic unit, the integrated  
10 circuit device 30 is attached to an insulating support 50 by means of a layer of adhesive material 52, the external face 54 of the insulating substrate being provided with external electrical contact pads 56. Windows such as window 58 are provided within the  
15 insulating substrate in front of each of pads 56. A lead wire 60, for example, made of gold, is attached, on the one hand, to the connection terminal 36 and, on the other hand, to the back face of an external electrical contact pad 56 through window 58. It should be  
20 understood that because of the very small thickness of active layer 32, terminals 36 are close to the insulating substrate 50. This allows for the whole bent lead wire 60 to be located below plane PP', which includes the upper face 44 of complementary layer 40.

25 The same would hold if the lead wires were replaced by elongated electrical connection elements.

In order to complete the electronic unit, the encapsulation 62 only needs to be formed, with its total thickness  $h$  reduced thanks to the above described  
30 provisions.

In the described implementation, the overall thickness  $h$  of the encapsulation is  $310\text{ }\mu\text{m}$  if thickness of the adhesive layer between the substrate and the integrated circuit device is taken into account. The  
35 thickness  $e_3$  of the insulating substrate being typically of  $170\text{ }\mu\text{m}$ , the obtained electronic unit has a thickness of  $480\text{ }\mu\text{m}$ . This represents a very large thickness reduction relative to standard electronic units.



Referring now to figures 4A, 4B and 4c, the main steps in the manufacture of integrated circuit device 30 will be explained.

5 In a first step shown in Figure 4A, a silicon wafer is diced by means of any appropriate method allowing the complementary layer 40 to be formed with its recesses 46. This layer could be made of any other material. Its thickness  $e_1$  preferably ranges from 100 to 200  $\mu\text{m}$ .

10 Then, in a step shown in Figure 4B, the complementary layer 40 is attached to the active face 72 of a semiconductor chip 50 provided with connection terminals 36. This chip has a standard thickness  $d$  of about 180  $\mu\text{m}$ .

15 Finally, in a step shown in Figure 4C, the non-active face 74 of chip 70 is processed by any appropriate method so as to reduce its thickness  $e_2$  to a typical value of 40  $\mu\text{m}$ , and active layer 32 is obtained.

20 Due to the presence of complementary layer 40, the integrated circuit device 30 has an overall thickness of about 180  $\mu\text{m}$  in the considered example. One thus obtains a component of sufficient mechanical strength although the active layer 32 by itself has a thickness  $e_2$  which does not provide such mechanical strength properties. Therefore, as already explained, the main advantage of  
25 the thus obtained component is that the contact terminals 36 are in very close proximity to the component attachment face 38.